REMARKS/ARGUMENTS

Reconsideration and allowance of this application are respectfully requested in view of the following remarks. Claims 24 and 25 have been amended to give greater emphasis to some of the novel and patentable features set forth in these claims. New dependent claims 27-32 have been added.

Independent claim 25 and dependent claims 5-7 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite. The Office Action alleges that the meaning of the term "non-embedded" in independent claim 25 is not clear. This rejection is respectfully traversed.

At the outset, Applicants' specification, in the "Background And Summary Of The Invention" section, sets forth the context of an "on-chip" memory verses an "external" frame buffer memory that is "part of the main memory of the graphics system" :

> "A problem graphics system designers confronted in the past was to provide a powerful yet inexpensive system which enables various data formats to be stored and processed thereby in a efficient and advantageous manner. Graphics chips used in graphics systems have included a *local or on-chip memory* for storing data as it is rendered by the graphics pipeline. When data is generated by the graphics chip it is transferred from the local memory *to an external memory*, where it can be used by, for example, a video interface unit to display the data on a display device. *This external memory is typically part of the main memory of the graphics system..."*
>
> --Applicants' specification at page 7, lines 9-16 (emphasis added)

Applicants' specification also clearly specifies "an embedded (on-chip) frame buffer memory 702" (at page 21, line 11). Moreover, Applicants' specification describes graphics pipeline 180 as including one or more "embedded" DRAM memories 702 for storing frame buffer information locally (page 21, lines 12-14) and refers to an "on-chip frame buffer 702" (page 21, line 17) in the context of being on the same semiconductor

"chip" as graphics coprocessor pipeline logic circuitry 180. (See Applicants' specification at page 21, lines 11-18.) In addition, Applicants' FIGURE 11 shows graphics chip 114 as having an "embedded frame buffer memory". Accordingly, from at least the context of this portion of the description in Applicants' specification, it should be clear to one skilled in the art that a "non-embedded ...memory", as recited in Applicants' claim, implies memory that is not on the same semiconductor "chip" as graphics coprocessor pipeline logic circuitry 180.

Claims 25, 5-7 and 24 stand rejected under 35 USC §103(a) as being obvious over Chen et al. (U.S. Patent 6,532,018) in view of Migdal (U.S. Patent No. 6,426,753). Claims 11, 21 and 26 stand rejected under 35 USC §103(a) as being obvious over Chen et al. ('018) in view of Migdal '753 and further in view of Nally (U.S. Patent No. 5,506,604) and dependent claims 17, 19, 20 and 22 stand rejected under 35 USC §103(a) as being obvious over Chen et al. in view of Nally et al. '604 and further in view of Nakamura et al. (U.S. Patent No. 6,384,831). In addition, independent claims 24 and 26 stand rejected under §102(e) as being anticipated by Yasumoto (U.S. Patent 6,747,642).

Applicants respectfully submit that independent claims 24, 25 and 26, as well as all claims dependent thereon, are not anticipated by or rendered obvious by the cited references or any prior art of record, for at least the following reasons:

Independent claim 24, as currently amended, recites a copy-out process that includes "creating texture tiles within said external texture buffer by converting a selected rectangular sub-region of pixels from a display data format to one of a plurality of texture data formats..." None of the prior art of record, considered alone or in

combination, discloses or suggests creating texture tiles from rectangular sub-region of pixels during a copy-out process. Moreover, independent claim 24, as currently amended, also recites a copy-out process from a frame buffer embedded on a same semiconductor chip substrate as at least a portion of a graphics processing pipeline to an "external texture buffer residing within a main memory of said graphics system, said main memory being configured on one or more semiconductor chips separate from a semiconductor chip containing said graphics processing pipeline". None of the prior art of record, considered alone or in combination, discloses or suggests performing a copy-out of pixel data to an external *texture* buffer located in an external main memory that is separate from a semiconductor chip containing graphics processing pipeline circuitry, as set forth in Applicants' claim 24.

Independent claim 25, as currently amended, recites "an associated graphics system main memory..., said graphics system main memory being separate memory that is not embedded on a same graphics coprocessor chip as graphics processing pipeline circuitry...wherein the copy-out pipeline is operable to selectively transfer the data to either a display buffer area or a texture buffer area within said separate non-embedded main memory and wherein the copy-out pipeline converts the data to a display format if the data is transferred to the display buffer area and converts the data to a texture format if the data is transferred to the texture buffer area." None of the prior art of record, considered alone or in combination, discloses or suggests a copy-out pipeline for copying pixel data to a separate main memory that is not embedded on a same graphics coprocessor chip as graphics processing pipeline circuitry and in which data is converted to either a texture format or a display format upon being selectively

copied out to either a display buffer area or a texture buffer area within the separate non-embedded main memory, as set forth in Applicants' claim 25.

Applicants' independent claim 26 recites:

> "A method of *reducing an amount of storage space required for storing image data in main memory in a graphics processing system while increasing main memory bandwidth* when displaying image data from a frame buffer *located in said main memory*, said graphics processing system including a graphics processing chip having an embedded first frame buffer memory *and a separate non-embedded second frame buffer in a main memory provided separate from said graphics processing chip*,..." (emphasis added)

None of the references of record, considered alone or in combination, teach or suggest converting the image data from an RGB format to a YUV display format to reduce the amount of storage space needed to store the image data in main memory and to provide an increase in main memory bandwidth when displaying image data from the graphics system main memory.

Moreover, independent claim 26 also recites "initiating a copy out operation for transferring image data from the first embedded frame buffer to the separate non-embedded second frame buffer located in the *main memory of the graphics system*" and "*converting* the image data *from an RGB format to a YUV display format during the copy out operation* between the embedded first frame buffer and the non-embedded second frame buffer...". Applicants contend that Chen et al.'s suggestion of performing *some* formatting prior to displaying on a monitor (See Chen et al. patent at column 2, lines 42-46.) does not anticipate or even suggest Applicants' claimed process of converting pixel data from an RGB format to a YUV display format during the copy out operation between an embedded frame buffer and a separate non-embedded main memory, as set forth in Applicants' claim 26.

Applicants also respectfully traverse the Office Action contention that Applicants' claimed feature of using a copy pipeline to transfer the data from an embedded frame buffer to an external system main memory would be obvious over Chen et al. in view of Migdal. Applicants contend that the cited passages relied upon in the '098 Chen et al. and Migdal patents at most suggest only the capability of *copying data to from one M chip to another M chip*, neither M chip of which comprises a part of the graphics system "main memory". Moreover, neither Chen et al. nor Migdal, considered either alone or together, teaches or suggests copying image data from an embedded frame buffer on a graphics processor chip *to a separate non-embedded main memory* of the graphics system, as set forth in Applicants' claim 26. In addition, Applicants contend that Chen et al. teaches away from Applicants' claimed arrangement for copying out image data to a separate non-embedded off-chip main memory, as evidenced by the Chen et al. '018 patent at column 2, lines 4-6 and lines 53-56, column 4, lines 48-50 and at column 5, lines 2-4, wherein Chen et al. explicitly states that "[T]he data never needs to leave the substrate."

The rejection of claims 25, 5-7 and 24 under 35 U.S.C. §103 as being unpatentable over Chen et al. ('018) in view of Migdal (753) and, in addition, the rejection of dependent claims 11, 21 and 26 as being obvious over Chen et al. ('018) in view of Migdal ('753) and further in view of Nally et al. (U.S. Patent No. 5,506,604), is respectfully traversed. For at least the following reasons:

Independent claim 25 recites a graphics system, comprising: a pixel data post-processing copy-out pipeline that selectively converts pixel data from one image format to another during a reading and transfer of the data from the embedded frame buffer to

a separate *non-embedded* main memory of said graphics system, wherein the copy-out pipeline is operable to selectively transfer the data *to either a display buffer area or a texture buffer area within said main memory* and wherein the copy-out pipeline *converts the data to a display format if the data is transferred to the display buffer area* and converts the data *to a texture format if the data is transferred to the texture buffer area.*

Applicants respectfully contend that the '018 Chen et al. reference fails to teach or suggest converting the image data to a display format if the data is transferred to a display buffer area and converting the image data to a texture format if the data is transferred to a texture buffer area, as set forth by independent claim 25. The '018 Chen et al. reference also fails to teach or suggest the above claimed features for at least the same reasons as set forth above with respect to independent claim 26.

Moreover, Applicants respectfully contend that the Migdal ('753) reference neither teaches nor suggests the above recited features of claim 25 either when considered alone or together with Chen et al. or any other reference of record. Migdal fails to teach or suggest a *copy-out pipeline* arrangement as claimed by Applicants. Instead, the Migdal '753 patent is directed toward a completely different architecture that uses a *distributed* frame buffer and texture cache memory arrangement accessed over a system network (102). Accordingly, Applicants respectfully contend that there is no teaching or suggestion by either Chen et al. or Migdal of a *copy-out pipeline* arrangement for a graphics system in which pixel data is copied from a frame buffer memory instantiated on the same semiconductor chip as a graphics coprocessor to a *separate non-embedded main memory* as set forth in Applicants' claims. In fact, the very nature of Migdal's distributed memory arrangement clearly teaches away from

Applicants' claimed arrangement *as there is no "main memory" per se* in Migdal's *distributed* memory arrangement and, moreover, there would be no need to copy-out data to such a separate main memory. When a rejection depends on a combination of prior art references, there must be some teaching, suggestion, or motivation to combine the references. See *In re Geiger*, 815 F. 2d 686, 688, 2 USPQ2d 1276, 1278 (Fed. Cir. 1987).

In addition, Applicants respectfully contend that there is no teaching by Migdal that would suggest the obviousness of modifying the system of Chen et al. to implement a copy-out pipeline or to provide a separate non-embedded main memory separate from Chen et al.'s combined logic and memory chip. Moreover, there is no teaching or suggestion by Migdal to selectively transfer data to either a display area buffer or a texture area buffer or to provide specific format conversions dependent upon whether the data is copied out to a display buffer area or a texture buffer area in main memory, as set forth in Applicants' claim 25. Applicants respectfully contend that the Office Action improperly relies on hindsight reconstruction of the claimed invention based on the teachings of the instant application in reaching its obviousness determination. "To imbue one of ordinary skill in the art with knowledge of the invention, when no prior art reference or references of record convey or suggest that knowledge, is to fall victim to the insidious effect of a hindsight syndrome wherein that which only the inventor taught is used against its teacher." See *W.L. Gore & Assoc. v. Garlock, Inc.*, 721 F.2d 1540, 1543, 220 USPQ 303, 312-13 (Fed. Cir. 1983). Only in view of the teachings of the instant application could the rejections possibly be maintained.

Likewise, although directed toward processing video data from a first YUV format to a second YUV format, the Nally et al. ('604) patent fails to make up for the deficiencies of the Chen et al. and Migdal references as discussed above. Accordingly, it is submitted that independent claims 24, 25 and 26 and claims 5-7, 11, 17 and 19-22 dependent thereon are patentably distinct over the combined teachings of Chen et al. ('018) in view of Migdal ('753) and/or further in view of Nally et al. ('604).

The rejection of dependent claims 17, 19, 20 and 22 as being obvious over Chen et al. in view of Nalley et al. and further in view of Nakamura et al. ('831) is also respectfully traversed. Nakamura et al. discloses, inter alia, a graphic processor system capable of computing a weighted average of pieces of pixel data. However, Nakamura et al. fail to make up for the deficiencies of the Chen et al. and Nalley et al. references for at least the same reasons as set forth above with respect to independent claim 26 from which they depend.

The rejection of claims 24 and 26 under 35 U. S. C. §102(e) as being anticipated by Yasumoto (U.S. Patent No. 6,747,642) is respectfully traversed. Yasumoto suggests only that "pixel filter 50 may operate to apply *border line cartoon outlining*" (emphasis added) but does not disclose (or suggest) creating texture tiles in an external *texture* buffer as set forth in Applicants' claim 24, or converting image data from an RGB format to a YUV display format during the copy-out operation, as set forth in Applicants' claim 26.

With respectful traverse, Applicants also wish to point out that the Yamamoto '642 patent does not disclose or suggest converting pixel data stored in a frame buffer in RGB format to a YUV display format during the copy-out process, as alleged by the

Office Action with reference to column 10, lines 33-40 of that patent. In fact, the Yamamoto '642 patent only suggests that in using the disclosed prescribed blending calculations it might be possible to achieve greater optimization of the selective blending process for rendering border line colors if a YUV color format were used for the pixel data instead of using an RGB format. (See '642 patent at col. 10, lines 37-40.) Applicants respectfully contend that the suggestion to use YUV data in the blending process for rendering border line colors does not imply nor suggest that a conversion from RGB to YUV be performed during the copy-out process. In fact, there would be no need to perform Applicants claimed conversion to YUV on copy-out if the pixel data used was already in YUV format.

For at least the above reasons, Applicants respectfully contend that the Yasumoto patent does not anticipate independent claims 24 and 25 because it does not disclose every element of the invention as claimed. See *Lewmar Marine, Inc. v. Barient, Inc.*, 3 U.S.P.Q. 2d 1766 (Fed. Cir. 1987).

Having fully responded to all of the pending objections and rejections contained in this Office Action, Applicants submit that all claims now remaining in the present application are in condition for allowance and earnestly solicit an early Notice to that effect. The Examiner is invited to contact the undersigned if any further information is required.

Respectfully submitted,

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